## CLAIMS

I claim:

1. An integrated circuit comprising:

a first conductor; and

a second conductor contacted to the first conductor through a metal plug, the first conductor having at least one dummy via plug disposed from the first conductor in a direction perpendicular to a plane of first conductor at a location site of atomic flux divergence.

2. The integrated circuit of claim 1 wherein the at least one dummy via plug is disposed underneath the first conductor and proximate to the metal plug.

3. The integrated circuit of claim 1 wherein the at least one dummy via plug is to provide a reservoir for metal ions to reduce electromigration-induced mechanical stress.

4. The integrated circuit of claim 1 wherein the at least one dummy via plug is to be electrically passive within the integrated circuit.

5. The integrated circuit of claim 1 wherein the location site of atomic flux divergence comprises at least one of an electrically active metal via, an electrically active metal trench, and a bend in the first conductor.

6. An integrated circuit comprising:

a first conductor; and

a second conductor contacted to the first conductor through a metal via plug, the first conductor having at least two dummy via plugs disposed in a vertical plane relative to a longitudinal axis of the first conductor at a location of the metal via plug.

7. The integrated circuit of claim 6 wherein the at least two dummy via plugs are to act as passive reservoirs for metal ions to reduce a build-up of electromigration-induced mechanical stress.

8. The integrated circuit of claim 6 wherein the at least two dummy via plugs are to be electrically passive within the integrated circuit.

9. A method comprising:

forming an inter-layer dielectric and following metallization layer on a substrate, the metallization layer comprising at least one first interconnect;

forming an upper inter-layer dielectric and an upper metallization layer over the inter-layer dielectric and the metallization layer, the upper metallization layer comprising at least one upper interconnect having a metal plug to contact the first interconnect; and

providing at least one dummy via plug disposed underneath the at least one first interconnect proximate to the metal plug.

10. The method of claim 9 wherein the at least one dummy via plug provides a reservoir for metal ions to reduce a build-up of electromigration-induced mechanical stress.

11. The method of claim 9 wherein the at least one dummy via plug is not in electrical contact with other interconnects within an integrated circuit.

12. The method of claim 9 wherein the first and upper interconnects include a conductive material selected from the group consisting of copper, silver and gold.

13. The method of claim 9 wherein the at least two dummy via plugs are provided underneath the at least one first interconnect and proximate to the metal plug.

14. A machine-readable medium that provides instructions, which when executed by a set of one or more processors, cause said set of processors to perform operations comprising:

forming a dummy via plug;

forming a first interconnect electrically connected to the dummy via plug at a particular location, where the dummy via plug is disposed from the interconnect in a direction perpendicular to the plane of the interconnect;

forming a second via plug electrically connected to the first interconnect near the particular location; and

forming a second interconnect electrically connected to the first interconnect through the second via plug.

15. The medium of claim 14, wherein:

forming the dummy via plug includes forming the dummy via plug such that the dummy via plug does not contact any active electrical circuit other than the first interconnect.

16. The medium of claim 14, wherein:

the dummy via plug is disposed underneath the first interconnect.